

A Comparative Analysis between GaN-Based Current and Voltage Mode Class-D and E PAs for Communications

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Abstract: This work implements three discrete switched mode power amplifier (PA) topologies, namely inverse class-D (CMCD), push-pull class-E, and inverse push-pull class-E, in a GaN-on-Si process for medium power level (5-10W) transmitters. The designs are analyzed and compared with respect to non-idealities such as bondwire effects and input signal duty cycle variation, for use with digitally modulated signals such as RFPWM. After comparing the three topologies, this work concludes that an inverse push-pull class-E architecture gives highest output power and efficiency for discrete GaN-based power amplifiers, and a voltage-mode class D PA gives an output power that is most responsive to varying input duty cycle. The presented inverse class-E PA achieves 61.5% drain efficiency at 37.7dBm output power in the 880MHz band.

Keywords: transmitters, power amplifiers, class E, class D, RFPWM

Introduction

With rapid progress in compound semiconductor structures like GaN/GaAs/InP, as well as the rapid evolution of digital processing technologies, the digital transmitter architecture employing a Switched-Mode Power Amplifier (SMPA) is becoming an increasingly more viable solution to meet the demands for RF transceiver programmability and efficiency. Radar and imaging systems that use constant envelope waveforms may exploit the advantages of highly nonlinear, or switched-mode amplifiers [1]. Furthermore, digital transmitters are appealing potential hardware solutions to address future convergence of RF communications and radar supported within the same RF transceiver hardware. One of the main challenges for realizing a digital transmitter is high efficiency implementation of the SMPA, which is the focus of this presented work.

SMPAs are known for efficient amplification of constant-envelope signals for radar, or communications such as GSM, GMSK. However, with non-constant envelope (reduced duty-cycles in an RFPWM architecture), the output power of the SMPA decreases, thus requiring SMPA architectures that can efficiently amplify reduced duty cycles at power back-off (PBO). In this work, three SMPA architectures have been implemented in a GaN-on-Si process for a medium power (5-10W) applications at 900MHz. These PAs are compared to one another with

respect to efficiency, maximum achievable output power for a fixed device size, and practical implementation constraints. Though GaN PAs have been demonstrated to give good performance at high power levels, it has been less investigated for low and medium power levels.

Overview of Switched-Mode PA Operation

In switched-mode power amplifiers, the transistor operates in triode and cut-off regions. As a result, there is very low current-voltage overlap. Theoretically SMPAs are 100% efficient, assuming an ideal transistor with zero knee voltage and zero on-resistance. However any transistor operating as a switch is non-ideal and has parasitic elements, which lead to losses and non-100% efficiency. When the switch is ON, finite switch on-resistance R_{ON} causes loss. When the switch makes an ON-to-OFF transition, parasitic series inductance L_s causes loss given as [2]:

$$P_{L_s} = \frac{L_s * I_{OFF}^2 * f}{2} \quad (1)$$

where P_{L_s} is the power loss due to parasitic series inductor, and I_{OFF} is the current through the switch just before turning ON. When the switch is making an OFF-to-ON transition, there is also loss associated with the charging and discharging of parasitic drain capacitance C_{DS} given as [2]:

$$P_{C_{DS}} = \frac{C_{DS} * V_{ON}^2 * f}{2} \quad (2)$$

where $P_{C_{DS}}$ is the power loss due to parasitic drain capacitance, and V_{ON} is the voltage across the switch just before turning off.

Class-E and Inverse Class-E Power Amplifiers: Class-E and inverse class-E SMPAs work on the principle of minimizing switching power consumption during the current-voltage overlap by applying two boundary conditions of zero voltage/current switching (ZVS/ZCS) and zero voltage/current derivative switching (ZVDS/ZCDS). This is accomplished by using a passive RLC load network known as the ZVS/ZCS network. The ZVS network ensures that the drain voltage is zero when the switch turns ON, while the ZCS network ensures that the drain current is zero when the switch is turned OFF. The RLC values can be chosen such that the voltage/current waveforms derivatives are also at zero

(ZVDS/ZCDS). Class E overcomes the turn-ON loss shown in Equation 2 by incorporating the parasitic drain capacitance C_{DS} , while inverse class-E overcomes the turn-OFF loss shown in Equation 1 by overcoming the parasitic drain inductance L_S . Hence, inverse class-E becomes more suitable for discrete PA realizations where the effect of bondwire inductance can exacerbate the effect of parasitic series drain inductance. In GaN-based PAs, the drain capacitance is relatively low, making inverse class-E a good choice.

The variation in output power and drain efficiency (η) of a class-E and inverse class-E PA with respect to duty cycle (D) was analyzed extensively in [3], [4], [5], [6]. It was shown that ZVDS/ZCDS is not necessary to obtain highest efficiency, and this “sub-optimal” architecture allows for more design flexibility [7]. Hence, sub-optimum class-E/inverse class-E designs were implemented in this work and compared with respect to reduced duty cycle performance. Although [8] theoretically discusses that inverse class-E is suited for signals with high amplitude modulation index, it has not been demonstrated so far. This work shows that inverse class-E undergoes less efficiency degradation under reduced duty cycle (power back-off) as compared to other SMPA topologies implemented in this work.

Class-D and Inverse Class-D Power Amplifiers: Though class-D amplifiers have conventionally been known to give high efficiency at audio frequencies, the switching losses given by Equations 1 and 2 cause tremendous efficiency degradation and there is no mechanism to counter these switching losses in a Voltage Mode Class D (VMCD) PA; therefore, efficiency and frequency of operation are limited. An inverse class-D amplifier, also known as a Current-Mode Class-D (CMCD) PA is a good alternative because the parasitic device capacitance can be incorporated into the output tank circuit to achieve ZVS during the switch turn-on. CMCDs are easier to realize because they do not require a complimentary device like single ended class-D, or a center tapped transformer as in a transformer coupled VMCD. CMCD is a push-pull amplifier, but can be implemented with a balun, which typically has lower insertion loss compared to a center tapped transformer.

Implemented Switched-Mode PA Topologies

Three SMPA topologies have been selected for 900MHz medium power applications using non-constant envelope input signals: CMCD (Figure 1), sub-optimal push-pull class-E (Figure 2), sub-optimal inverse push-pull class-E (Figure 3). In addition to the three implemented architectures, a VMCD PA was also simulated for comparison. These PAs have been implemented using 4mm GaN-on-Si discrete devices with 200 μ m length. The devices are wirebonded to a PCB. These devices were custom modeled to include self-heating effects and enable transient simulations. Since the design was targeted for medium power (5-7W) applications, a 10V supply was

chosen. The duty cycle was varied and plotted against output power and drain efficiency in Figures 4 and 5. Table I summarizes PA simulation results for 50% duty cycle.

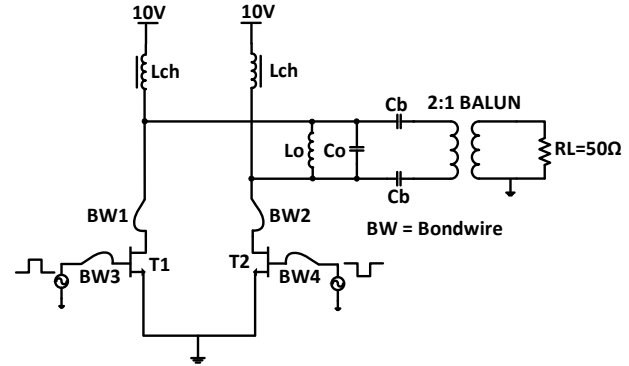


Figure 1. Implemented Current-Mode Class-D PA.

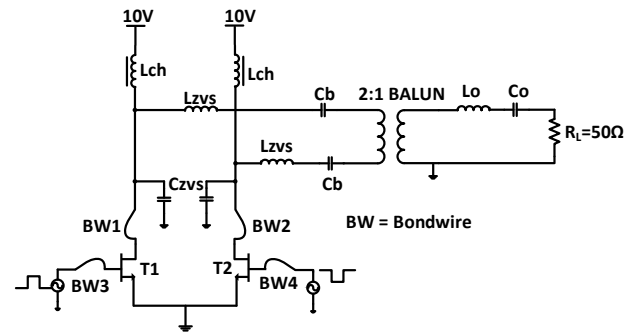


Figure 2. Implemented Push-Pull Class-E PA.

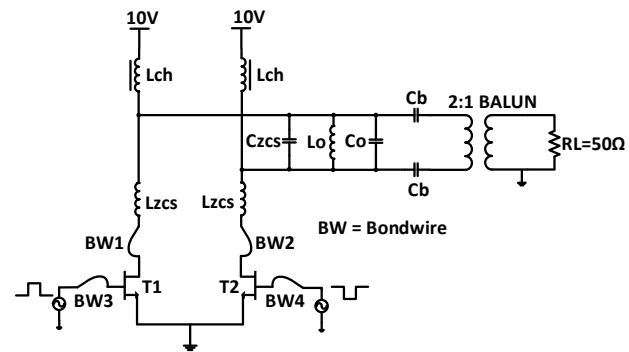


Figure 3. Implemented Inverse Push-Pull Class-E PA.

The efficiency flatness of the inverse class-E power amplifier is always more than class-E and CMCD. With bondwire inductances, the PA must mitigate losses due to both L_S and C_{DS} . Since the losses due to bondwires dominate over C_{DS} losses (C_{DS} being lower in GaN), inverse class-E can obtain higher output power at higher efficiency compared to class-E and CMCD. Even though VMCD does not undergo much efficiency degradation under reduced duty cycle conditions, its efficiency is quite

low as compared to other topologies implemented in this work. The three implemented topologies have PBO efficiency comparable to the maximum VMCD efficiency. Hence, the presented architectures have good potential for efficiently amplifying varying pulse width (duty-cycle) input waveforms.

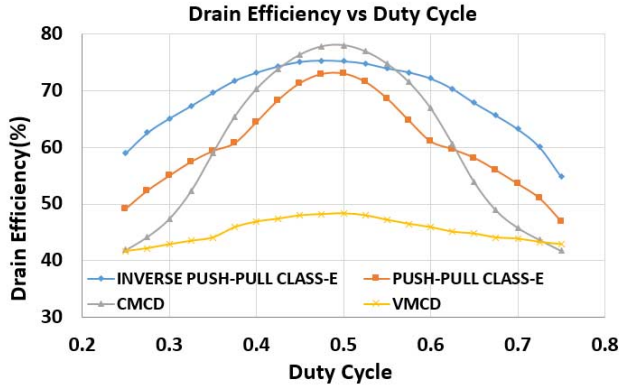


Figure 4. Simulated PA Drain Efficiency vs. Input Duty-Cycle.

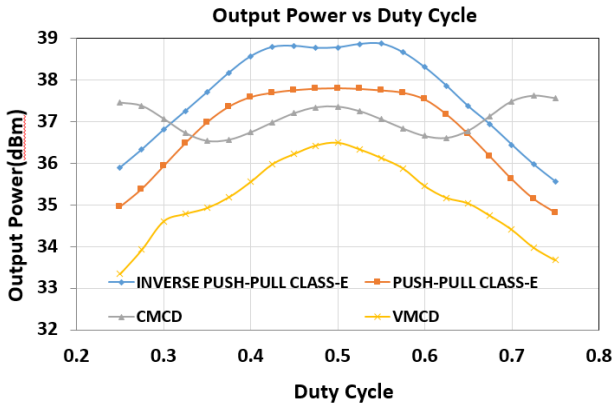


Figure 5. Simulated PA Output Power vs. Input Duty-Cycle.

Table 1. SMPA Simulation Results at 50% Duty Cycle

PA Topology	DE(%)	Saturated Output Power(dBm)
VMCD	49.2	36.5
CMCD	72.1	37.4
Push-pull class E	73	37.8
Inverse Push-pull class E	75.2	39.2

Measurement Results

Experimental Setup: The three SMPA topologies mentioned in the previous section were implemented by wire bonding two 4mm Nitronex GaN-on-Si die in the form of a differential pair on a two layer board of FR4 substrate. A 2:1 low insertion loss discrete balun by Anaren Microwave was used to achieve the impedance

transformation of the optimum load to a 50 ohm antenna load, thus avoiding an output L-match. Figure 6 shows the power amplifier board. The SMPA board was measured with 50% “square wave” inputs, emulated using an overdriven sine wave. A laboratory linear amplifier by was used to overdrive the input sine wave from the signal generator. The SMPA input signal was converted into differential inputs using a broadband balun from Hyperlabs.

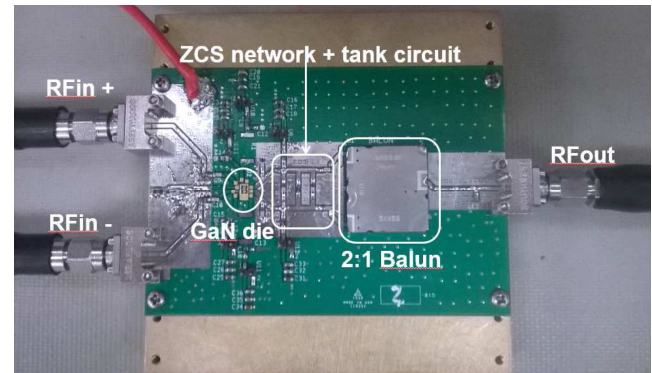


Figure 6. Implemented SMPA photo, showing the GaN die assembled with the on-board passive components, including the balun. This design is the inverse push-pull class E PA.

Results: Table 2 summarizes measured power amplifier performance. It is observed that the power amplifiers drift from the designed 900MHz and give better performance close to 880MHz for inverse push-pull class-E and push-pull class-E, and 860MHz for CMCD. The measurement results closely match simulation results. The power amplifiers maintain performance over a 60-80 MHz bandwidth, as shown in Figures 7 and 8.

Table 2. SMPA Measurement Results

PA Topology	DE(%)	Saturated Output Power(dBm)	Freq (MHz)
CMCD	63.8	35.8	864
Push-pull class E	61.4	36.3	874
Inverse Push-pull class E	61.5	37.7	878

Conclusion

Inverse push-pull class-E, push-pull class-E, and current-mode Class-D PAs have been implemented and measured in this work. The inverse class E PA achieves 61.5% efficiency for medium power levels (37.7dBm) at 880MHz. The three designed PAs have been compared with respect to duty-cycle variation in simulation. The inverse push-pull class-E power amplifier is an efficient option for GaN based discrete power amplifiers because it can incorporate the bondwire inductance and it is resilient to duty-cycle variations. This architecture is able to deliver high power at

high efficiencies. For systems with low parasitic series inductance, where low drain parasitic capacitance is the dominant cause of switching loss, Push-pull class-E and CMCD are the best suited switched-mode PA options. Unfortunately, these resonant-based amplifiers have output power that is less sensitive to duty-cycle variation than the voltage-mode class D. The measurements show that the sensitivity of the tuning network and complexity in implementation don't allow the class-E, inverse class-E, and CMCD to respond well to varying duty cycle.

In future work, supply regulation and alternative resonant topologies will be explored as methods to increase output power sensitivity to duty cycle without degrading efficiency.

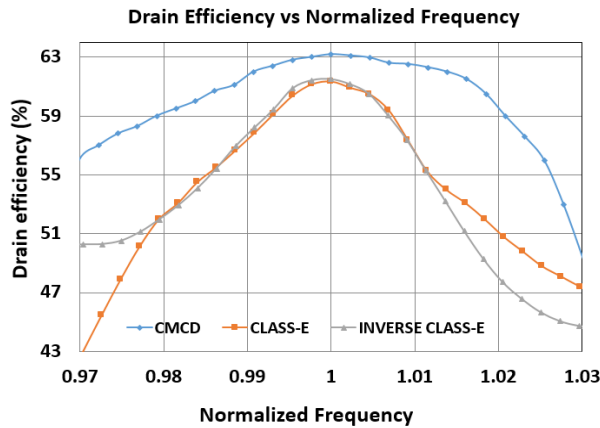


Figure 7. SMPA Drain Efficiency vs. Normalized Frequency.

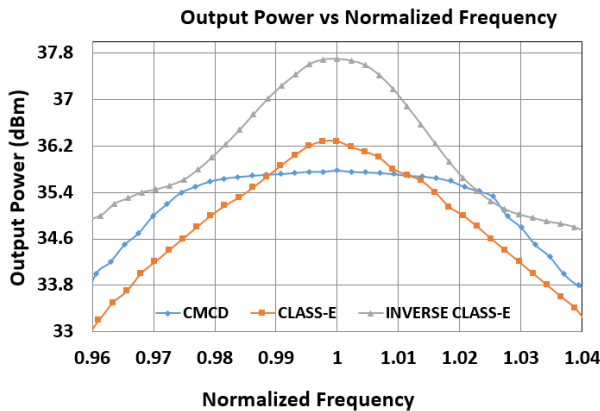


Figure 8. SMPA Output Power vs. Normalized Frequency.

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